**Advanced VLSI Design Project (Assigned 3/7/2016)**

1. Design a 32 bit ripple carry adder which adds two 32 bit positive integers. The adder produces a 33 bit sum. The input to the adder is captured in 64 flip-flops and output is supplied to 33 flip-flops. All input and output flip-flops are controlled by a common system clock.
2. Design 32 bit pipeline ripple carry adders that perform the same function as the original adder. Vary the number of pipeline stages as 2, 4, 8, 16 and 32. Study clock frequency, latency, throughput, and energy per cycle as functions of pipeline stages.

Your designs must satisfy the following conditions:

1. Designs can use any technology file from the PTM (predictive technology model) website (<http://ptm.asu.edu/>) as long as it is 45nm technology or better.
2. Your adders must work at the fastest possible clock without malfunctioning. You should be able to show the fastest possible clock by monitoring the critical path timing.
3. You may apply 100 random vectors to your adder at the fastest clock and calculate the total power dissipated. All designs must use the same 100 patterns, which should include a vector pair that activates the critical path.

Submit a project report in an IEEE paper format. **(Due 4/11/2016)**

1. Highlight the key differences in each design approach.
2. Compare and contrast the advantages and disadvantages of each design.
3. Comment on each adder's area, timing, and power overhead. Provide brief reasons for why results are as expected or not as expected.
4. In your conclusion, summarize what you have learned from the project, identify what you would have done differently if you were to do the project again, and what future direction you would want to take your project if you were given more time.
5. Prepare a 15-minute class presentation on the highlights of your project by summarizing results and conclusions.